Claims

[c1]   1.An ExpressCard comprising:

an ExpressCard connector for mating with a host Ex-

pressCard connector on a host;

a first flash-memory chip for storing data;

a second flash-memory chip for storing data;

a controller chip, coupled to the ExpressCard connector,

for controlling communication to the host through the

ExpressCard connector;

a first flash-memory channel between the controller chip

and the first flash-memory chip, the first flash-memory

channel having a first data bus for communicating data

between the controller chip and the first flash-memory

chip;

a second flash-memory channel between the controller

chip and the second flash-memory chip, the second

flash-memory channel having a second data bus for

communicating data between the controller chip and the

second flash-memory chip;

a shared control bus between the controller chip and the

first and second flash-memory chips;

a first response line from the first flash-memory chip to

the controller chip for indicating completion of an oper-

ation by the first flash-memory chip; and

a second response line from the second flash-memory chip to the controller chip for indicating completion of an operation by the second flash-memory chip, whereby the ExpressCard has two channels to the first and second flash-memory chips but a shared control bus to the first and second flash-memory chips.

[c2]   2.The ExpressCard of claim 1 further comprising:
a housing for enclosing the controller chip and the first and second flash-memory chips;
wherein the housing has an opening on an insertion end for the ExpressCard connector.

[c3]   3.The ExpressCard of claim 2 wherein the housing contains a cutout notch wherein a first width of the insertion end containing the ExpressCard connector is narrower than a second width of an opposite end that is opposite the insertion end.

[c4]   4.The ExpressCard of claim 2 wherein the first response line carries a ready signal from the first flash-memory chip;
wherein the second response line carries a ready signal from the second flash-memory chip,
whereby separate ready signals are sent to the controller chip.

[c5]   5. The ExpressCard of claim 4 wherein the controller chip
        further comprises:
        a serial engine, coupled to the ExpressCard connector,
        for sending and receiving serial signals representing data
        and commands from the host;
        a flash-memory controller for generating control signals
        on the shared control bus to the first and second flash-
        memory chips;
        a central processing unit (CPU) for executing routines of
        instructions to transfer data between the serial engine
        and the flash-memory controller.

[c6]   6. The ExpressCard of claim 5 wherein the controller chip
        further comprises
        an internal bus between the CPU, the serial engine, and
        the flash-memory controller.

[c7]   7. The ExpressCard of claim 5 wherein the controller chip
        further comprises:
        a system buffer for temporarily storing data transferred
        between the serial engine and the flash-memory con-
        troller;
        a scratch-pad random-access memory (RAM) for storing
        parameters used by the CPU; and
        a read-only memory (ROM) for storing the routines of in-
        structions executed by the CPU.

[c8] 8.The ExpressCard of claim 5 wherein the controller chip further comprises:

an error-correction code (ECC) generator, coupled to the flash-memory controller, for appending ECC bits to data being written to the first or second flash-memory chips, and for reading ECC bits and correcting errors in data read from the first or second flash-memory chips, whereby data errors are corrected by error-correction code.

[c9] 9.The ExpressCard of claim 5 wherein the routines of in-structions include routines to erase, read, or write data in the first or second flash-memory chips.

[c10] 10.The ExpressCard of claim 9 wherein the controller chip further comprises:

an input-output interface for driving an indicator lamp when the flash-memory controller is reading or writing to the first or second flash-memory chips.

[c11] 11.The ExpressCard of claim 5 wherein the shared con-trol bus comprises a read-enable signal and a write-enable signal that are connected to both the first and second flash-memory chips.

[c12] 12.The ExpressCard of claim 11 wherein the shared con-trol bus further comprises:

a command latch enable signal to latch a command into the first or second flash-memory chips;

an address latch enable signal to latch an address into the first or second flash-memory chips.

[c13] 13. The ExpressCard of claim 12 wherein the shared control bus comprises a shared chip-select signal to enable the first flash-memory chip and the second flash-memory chip.

[c14] 14. The ExpressCard of claim 5 wherein the ExpressCard connector has a pair of differential data lines for communicating data and commands from the host to the controller chip.

[c15] 15. The ExpressCard of claim 14 wherein the pair of differential data lines comprise Universal-Serial-Bus (USB) data lines, wherein the controller chip is a USB slave and the host is a USB host.

[c16] 16. A flash-storage ExpressCard comprising:

connector means for connecting to a host;

controller means for performing control functions;

flash-memory means for storing data in non-volatile memory;

a first channel between the controller means and the flash-memory means, the first channel having a first

data bus and a first ready means for indicating when a first flash-memory chip in the flash-memory means is busy;

a second channel between the controller means and the flash-memory means, the second channel having a second data bus and a second ready means for indicating when a second flash-memory chip in the flash-memory means is busy;

shared control bus means for sending flash control signals to flash-memory means;

flash-control means, in the controller means, for generating the flash control signals to the shared control bus means; and

serial control means, in the controller means, for serially communicating with the host through the connector means.

[c17]   17.The flash-storage ExpressCard of claim 16 wherein the serial control means comprises a Universal-Serial-Bus (USB) controller, and wherein the connector means includes a differential pair of serial data lines that carry serial USB signals between the host and the controller means, or

wherein the serial control means comprises a Peripheral Component Interconnect (PCI) Express controller, and wherein the connector means includes a differential pair

of PCI-Express-transmit serial data lines and a differential pair of PCI-Express-receive serial data lines that carry serial signals between the host and the controller means.

[c18] 18.The flash-storage ExpressCard of claim 16 wherein the serial control means comprises both a Universal-Serial-Bus (USB) controller, and a Peripheral Component Interconnect (PCI) Express controller;
and wherein the connector means includes a differential pair of serial data lines that carry serial USB signals between the host and the controller means when using the USB controller, and a differential pair of PCI-Express-transmit serial data lines and a differential pair of PCI-Express-receive serial data lines that carry serial signals between the host and the controller means when using the PCI Express controller,
whereby dual serial controllers allow communication with the host using either USB or PCI Express.

[c19] 19.An interleaved flash ExpressCard comprising:
an ExpressCard connector for plugging into a host;
a controller chip that has a microprocessor core, a program memory, a buffer memory, a serial controller, and a flash controller;
a first flash-memory chip in a first channel;
a second flash-memory chip in the first channel;

a third flash-memory chip in the first channel;

a fourth flash-memory chip in the first channel;

a shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the first, second, third, and fourth flash-memory chips;

a first data bus between the controller chip and the first and third flash-memory chip;

a first shared ready signal generated by the first flash-memory chip and the second flash-memory chip and driven to the controller chip;

a second data bus between the controller chip and the second and fourth flash-memory chip; and

a second shared ready signal generated by the third flash-memory chip and the fourth flash-memory chip and driven to the controller chip;

a first chip select generated by the controller chip and connected to the first and second flash-memory chip;

a second chip select generated by the controller chip and connected to the third and fourth flash-memory chip;

wherein the serial controller in the controller chip is a Universal-Serial-Bus (USB) controller that communicates to the host using a pair of differential USB data signals in the ExpressCard connector, or the serial controller in the controller chip is a Peripheral Component Interconnect (PCI) Express controller, a Firewire controller, a serial

ATA controller, or a serial small-computer system interface (SCSI) controller;

wherein access to the first and third flash-memory chips is interleaved;

wherein access to the second and fourth flash-memory chips is interleaved.

[c20] 20.An interleaved dual-channel flash ExpressCard comprising:

an ExpressCard connector for plugging into a host;

a controller chip that has a microprocessor core, a program memory, a buffer memory, a serial controller, and a flash controller;

a first flash-memory chip in a first channel;

a second flash-memory chip in a second channel;

a third flash-memory chip in the first channel;

a fourth flash-memory chip in the second channel;

a first shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the first and third flash-memory chips;

a first data bus between the controller chip and the first and third flash-memory chip;

a first ready signal generated by the first flash-memory chip and driven to the controller chip;

a third ready signal generated by the third flash-memory

chip and driven to the controller chip;

a second shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the second and fourth flash-memory chips;

a second data bus between the controller chip and the second and fourth flash-memory chip; and

a second ready signal generated by the second flash-memory chip and driven to the controller chip; and

a fourth ready signal generated by the fourth flash-memory chip and driven to the controller chip;

wherein the serial controller in the controller chip is a Universal-Serial-Bus (USB) controller that communicates to the host using a pair of differential USB data signals in the ExpressCard connector, or the serial controller in the controller chip is a Peripheral Component Interconnect (PCI) Express controller, a Firewire controller, a serial ATA controller, or a serial small-computer system interface (SCSI) controller,

wherein access to the first and third flash-memory chips is interleaved;

wherein access to the second and fourth flash-memory chips is interleaved.